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UTILITY PATENT APPLICATION TRANSMITTAL <small>(Only for new nonprovisional applications under 37 CFR 1.53(b))</small>	Attorney Docket No.	MI22-1114	Total Pages	51
	First Named Inventor or Application Identifier			
	Gurtej S. Sandhu et al.			
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APPLICATION ELEMENTS <small>See MPEP chapter 600 concerning utility patent application contents.</small>	ADDRESS TO: Assistant Commissioner for Patents Box Patent Application Washington, DC 20231
<p>1. <input checked="" type="checkbox"/> Fee Transmittal Form <small>(Submit an original, and a duplicate for fee processing)</small></p> <p>2. <input checked="" type="checkbox"/> Specification <small>[Total Pages 30]</small> <small>(preferred arrangement set forth below)</small></p> <ul style="list-style-type: none"> - Descriptive title of the Invention <u>PLUS TITLE PAGE</u> - Cross References to Related Applications - Statement Regarding Fed sponsored R & D - Reference to Microfiche Appendix - Background of the Invention - Brief Summary of the Invention - Brief Description of the Drawings (if filed) - Detailed Description - Claim(s) - Abstract of the Disclosure <p>3. <input checked="" type="checkbox"/> Drawing(s) (35 USC 113) <small>[Total Sheets 7]</small> <u>FIGS. 1-19</u></p> <p>4. Oath or Declaration <small>[Total Pages 3]</small></p> <ul style="list-style-type: none"> a. <input type="checkbox"/> Newly executed (original or copy) b. <input checked="" type="checkbox"/> Copy from a prior application (37 CFR 1.63(d)) <small>(for continuation/divisional with Box 17 completed)</small> <small>[Note Box 5 below]</small> <ul style="list-style-type: none"> i. <input type="checkbox"/> DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b). <p>5. <input checked="" type="checkbox"/> Incorporation By Reference (useable if Box 4b is checked) The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.</p>	<p>6. <input type="checkbox"/> Microfiche Computer Program (Appendix)</p> <p>7. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)</p> <ul style="list-style-type: none"> a. <input type="checkbox"/> Computer Readable Copy b. <input type="checkbox"/> Paper Copy (identical to computer copy) c. <input type="checkbox"/> Statement verifying identity of above copies
ACCOMPANYING APPLICATION PARTS	
<p>8. <input type="checkbox"/> Assignment Papers (cover sheet & document(s))</p> <p>9. <input type="checkbox"/> 37 CFR 3.73(b) Statement <input type="checkbox"/> Power of Attorney <small>(when there is an assignee)</small></p> <p>10. <input type="checkbox"/> English Translation Document (if applicable)</p> <p>11. <input checked="" type="checkbox"/> Information Disclosure Statement (IDS)/PTO-1449 <input type="checkbox"/> Copies of IDS Citations</p> <p>12. <input checked="" type="checkbox"/> Preliminary Amendment</p> <p>13. <input checked="" type="checkbox"/> Return Receipt Postcard (MPEP 503) <small>(Should be specifically itemized)</small></p> <p>14. <input type="checkbox"/> Small Entity <input type="checkbox"/> Statement filed in prior application, Status still proper and desired</p> <p>15. <input type="checkbox"/> Certified Copy of Priority Document(s) <small>(if foreign priority is claimed)</small></p> <p>16. <input checked="" type="checkbox"/> Other: <u>Change of Corres. Address</u> <u>Check for \$1,210; Fee Transmittal</u> <u>Formal Drawings</u></p>	

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☐ Continuation ☒ Divisional ☐ Continuation-in-part (CIP) of prior application No: 08/748,997

18. CORRESPONDENCE ADDRESS

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EL169865199

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PRIORITY Application Serial No. 08/748,997
PRIORITY Filing Date November 14, 1996
Inventor Gurtej S. Sandhu et al.
Assignee Micron Technology, Inc.
PRIORITY Group Art Unit 1765
PRIORITY Examiner Felisa C. Hiteshew
Attorney's Docket No. MI22-1114
Title: Method Of Forming A Crystalline Phase Material

PRELIMINARY AMENDMENT

To: Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

From: Mark S. Matkin (Tel. 509-624-4276; Fax 509-838-3424)
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Sir:

Please enter the following amendments prior to examining the
above-identified application. Applicant amends and remarks as follows:
[unless otherwise indicated, deletions are bracketed, additions are
underlined].

AMENDMENTS

In the Specification

At p. 1 before the "Technical Field" section, please insert the
following:

1 **--RELATED PATENT DATA**

2 This patent resulted from a divisional application of U.S. Patent
3 Application Serial No. 08/748,997, filed November 14, 1996, entitled
4 "Method Of Forming A Crystalline Phase Material", naming Gurtej S.
5 Sandhu and Sujit Sharan as inventors, and which is now U.S. Patent No.
6 _____, the disclosure of which is incorporated by reference.--

7
8 **In the Claims**

9 Please cancel claims 1-9 and 11-20 without prejudice.
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REMARKS

This application is a divisional application of U.S. Patent Application Serial No. 08/748,997. Claims 1-9 and 11-20 have been canceled without prejudice. Claims 10 and 21-51 remain in the application for consideration.

Respectfully submitted,

Dated:

4/18/99

By:

Mark S. Matkin

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EM057275775

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

* * * * *

Method of Forming A Crystalline Phase Material

* * * * *

INVENTORS

Gurtej S. Sandhu
Sujit Sharan

ATTORNEY'S DOCKET NO. MI22-510

EL169865199

658770-4-EE250

1 **TECHNICAL FIELD**

2 This invention relates generally to formation of crystalline phase
3 materials in semiconductor wafer processing and more particularly to
4 formation of refractory metal silicides and crystalline phase
5 transformation thereof.
6

7 **BACKGROUND OF THE INVENTION**

8
9 Silicides, such as titanium silicide and tungsten silicide, are
10 commonly utilized electrically conductive materials in semiconductor wafer
11 integrated circuitry fabrication. Such materials are utilized, for example,
12 as capping layers over underlying conductively doped polysilicon material
13 to form electrically conductive lines or interconnects. Such silicide
14 materials are also utilized at contact bases intermediate an underlying
15 silicon substrate and overlying conductive polysilicon contact plugging
16 material. Silicides can be provided by chemical vapor deposition, or by
17 deposition of elemental titanium or tungsten over an underlying silicon
18 surface. Subsequent high temperature annealing causes a chemical
19 reaction of the tungsten or titanium with the underlying silicon to form
20 the silicide compound.

21 Titanium silicide (TiSi_2) occurs in two different crystalline
22 structures or phases referred to as the C49 and C54 phase. The C49
23 structure is base-centered orthorhombic, while the C54 is face-centered
24 orthorhombic. The C54 phase occurs in the binary-phase diagram while

the C49 phase does not. The C49 phase is therefor considered to be metastable. The C54 phase is a densely packed structure having 7% less volume than the C49 phase. The C54 phase also has lower resistivity (higher conductivity) than the C49 phase.

The C49 phase forms at lower temperatures during a typical refractory metal silicide formation anneal (i.e. at from 500°C - 600°C) and transforms to the C54 phase at higher elevated temperatures (i.e., greater than or equal to about 650° C). The formation of the higher resistive C49 phase has been observed to be almost inevitable due to the lower activation energies associated with it (2.1 - 2.4 eV) which arises from the lower surface energy of the C49 phase compared to that of the more thermodynamically stable C54 phase. Hence, the desired C54 phase can be obtained by transforming the C49 phase at elevated temperatures.

Due at least in part to its greater conductivity, the C54 phase is much more desirable as contact or conductive line cladding material. Continued semiconductive wafer fabrication has achieved denser and smaller circuitry making silicide layers thinner and narrower in each subsequent processing generation. As the silicide layers become thinner and narrower, the ratio of surface area to volume of material to be transformed from the C49 to the C54 phase increases. This requires ever increasing activation energies to cause the desired transformation, which translates to higher anneal temperatures to effect the desired phase transformation. In some instances, the temperature must be at

1 least equal to or greater than 800° C. Unfortunately, heating a silicide
2 layer to a higher temperature can result in undesired precipitation and
3 agglomeration of silicon in such layer, and also adversely exposes the
4 wafer being processed to undesired and ever increasing thermal
5 exposure. The processing window for achieving or obtaining low
6 resistance silicide phases for smaller line widths and contacts continues
7 to be reduced, making fabrication difficult.

8 It would be desirable to develop methods which facilitate the C49
9 to C54 phase transformation in titanium silicide films. Although the
10 invention was developed with an eye towards overcoming this specific
11 problem, the artisan will appreciate applicability of the invention in
12 other areas, with the invention only being limited by the accompanying
13 claims appropriately interpreted in accordance with the Doctrine of
14 Equivalents.

15 16 17 SUMMARY

18 In but one aspect, the invention provides a method of forming a
19 crystalline phase material. In one implementation, the method is
20 performed by providing a stress inducing material within or operatively
21 adjacent a crystalline material of a first crystalline phase prior to
22 anneal. The crystalline material of the first crystalline phase is
23 annealed under conditions effective to transform it to a second
24 crystalline phase. The stress inducing material preferably induces

compressive stress within the first crystalline phase during the anneal to the second crystalline phase to lower the required activation energy to produce a more dense second crystalline phase.

In accordance another aspect, the invention provides a method of forming a refractory metal silicide. In one implementation, the method is performed by forming a refractory metal silicide of a first crystalline phase. Compressive stress inducing atoms are provided within the refractory metal silicide of the first crystalline phase, with the compressive stress inducing atoms being larger than silicon atoms of the silicide. With the compressive stress inducing atoms within the first phase refractory metal silicide, the refractory metal silicide of the first crystalline phase is annealed under conditions effective to transform said silicide to a more dense second crystalline phase.

In another implementation, a stress inducing material is formed over the opposite side of the wafer over which the first phase crystalline material is formed.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic sectional view of a semiconductor wafer fragment at one processing step in accordance with the invention.

1 Fig. 2 is a view of the Fig. 1 wafer at a processing step
2 subsequent to that shown by Fig. 1.

3 Fig. 3 is a diagrammatic sectional view of another alternate
4 semiconductor wafer fragment at an alternate processing step in
5 accordance with the invention.

6 Fig. 4 is a view of the Fig. 3 wafer at a processing step
7 subsequent to that shown by Fig. 3.

8 Fig. 5 is a diagrammatic sectional view of yet another alternate
9 semiconductor wafer fragment at another alternate processing step in
10 accordance with the invention.

11 Fig. 6 is a view of the Fig. 5 wafer at a processing step
12 subsequent to that shown by Fig. 5.

13 Fig. 7 is a diagrammatic sectional view of still another alternate
14 semiconductor wafer fragment at another alternate processing step in
15 accordance with the invention.

16 Fig. 8 is a view of the Fig. 7 wafer at a processing step
17 subsequent to that shown by Fig. 7.

18 Fig. 9 is a view of the Fig. 7 wafer at a processing step
19 subsequent to that shown by Fig. 8.

20 Fig. 10 is a diagrammatic sectional view of another alternate
21 semiconductor wafer fragment at another alternate processing step in
22 accordance with the invention.

23 Fig. 11 is a view of the Fig. 10 wafer at a processing step
24 subsequent to that shown by Fig. 10.

Fig. 12 is a view of the Fig. 10 wafer at a processing step subsequent to that shown by Fig. 11.

Fig. 13 is a diagrammatic sectional view of another alternate semiconductor wafer fragment at another alternate processing step in accordance with the invention.

Fig. 14 is a view of the Fig. 13 wafer at a processing step subsequent to that shown by Fig. 13.

Fig. 15 is a view of the Fig. 13 wafer at a processing step subsequent to that shown by Fig. 14.

Fig. 16 is a view of the Fig. 13 wafer at a processing step subsequent to that shown by Fig. 15.

Fig. 17 is a diagrammatic sectional view of still another alternate semiconductor wafer fragment at another alternate processing step in accordance with the invention.

Fig. 18 is a view of the Fig. 17 wafer at a processing step subsequent to that shown by Fig. 17.

Fig. 19 is a view of the Fig. 17 wafer at a processing step subsequent to that shown by Fig. 18.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring initially to Figs. 1 and 2, a semiconductor wafer fragment in process is indicated generally with reference numeral 10. Such comprises a substrate 12, for example in the form of a bulk monocrystalline silicon wafer, having an overlying crystalline material layer 14 capable of undergoing a phase transformation from a first crystalline phase to a second crystalline phase. Example materials include refractory metal silicides, such as TiSi_x (where "x" ranges from 0.5 to 2.5 and is predominately "2") with a first crystalline phase being C49 and a second crystalline phase being C54. In the context of this document, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

A layer 16 of compressive stress inducing material is provided over and in contact with (i.e., "on") first crystalline phase material 14. Layer 16 ideally has a thermal coefficient of expansion which is less

1 than the thermal coefficient of expansion of first crystalline phase
 2 material layer 14, particularly at a desired temperature of phase
 3 transformation. Thus, the stress induced in layer 14 at phase
 4 transformation anneal will be of a compressive nature due to the
 5 greater expansion properties of layer 14 as compared to those of layer
 6 16. Layer 16 preferably has a thickness which is equal to or greater
 7 than a thickness of first phase crystalline material 14 to facilitate
 8 inducing desired stress. An example thickness for layers 14 and 16 is
 9 from 100 to 2000 Angstroms. Layer 16 is preferably comprised of a
 10 material that will not react with the underlying refractory metal silicide.
 11 Example and preferred materials for layer 16 include SiO_2 (doped or
 12 undoped) and Si_3N_4 .

13 Referring to Fig. 2, first phase crystalline material layer 14 is
 14 annealed under conditions effective to transform it to a second more
 15 dense and electrically conductive crystalline phase layer 15, such as C54
 16 TiS_x in the case of C49 titanium silicide of layer 14. The phase
 17 transformation of a refractory metal silicide from the C49 phase to the
 18 C54 phase occurs with the 7% volume reduction or density increase.
 19 Compressive stresses induced by the lesser expanding layer 16 during
 20 anneal help to facilitate phase transformation from C49 to C54 by the
 21 compressive forces facilitating this volume reduction, and reduces the
 22 required activation energy for achieving the phase transformation, which
 23 is typically in the prior art provided by temperature anneal alone. For
 24 example, one prior art processing window for achieving the desired

1 phase transformation is at a temperature of 800° C for a tightly
2 controlled period of time of from 15 - 20 seconds for a 350 Angstrom
3 thick C49 TiSi_x film. Utilizing a compressive stress inducing layer 16
4 enables transformation to occur at temperatures less than or equal to
5 about 750° C in an inert atmosphere (i.e., nitrogen or argon) and with
6 less stringent time requirements, and thus potentially enables less
7 thermal processing of the substrate being treated. An example pressure
8 during the anneal would be from 1 Torr to 760 Torr.

9 The above first described preferred embodiment is but one
10 example of a method of providing a stress inducing material (i.e.,
11 layer 16) operatively adjacent a crystalline material of a first crystalline
12 phase (i.e. layer 14) to be effective to induce stress (i.e. in this
13 example compressive stress) as the material is annealed to a second
14 crystalline phase. An alternate example of providing a stress inducing
15 material operatively adjacent a crystalline material to be transformed to
16 a secondary crystalline phase is to provide such stress inducing material
17 under or inwardly of the first crystalline phase material, as described
18 with reference to Figs. 3 - 4. Such illustrates a semiconductor wafer
19 fragment in process generally with reference numeral 18. In Fig. 3,
20 such comprises a substrate 20, for example bulk monocrystalline silicon
21 or layers of material, having an overlying stress inducing material
22 layer 22. A layer 24 of crystalline material of the first crystalline
23 phase is provided outwardly of layer 22, with layer 22 thus being
24 inwardly of or under layer 24 and in the illustrated example in contact

therewith. In the example refractory metal silicide transformation of a C49 phase to a C54 phase accompanied by a volume reduction, layer 22 ideally also has a coefficient of expansion which is less than the coefficient of expansion of layer 24. Such facilitates putting layer 24 in compressive stress during phase transformation. Example materials include those provided above for layer 16.

Referring to Fig. 4, annealing is conducted as in the first described embodiment to transform first crystalline phase material layer 24 into a more dense and higher electrically conductive second phase material layer 25.

Yet another alternate example is described with reference to Figs. 5 and 6. Here, the stress inducing material is provided within the crystalline material undergoing phase transformation. Fig. 5 illustrates a wafer fragment 30 comprised of some substrate construction 32. Again, such could be a monocrystalline silicon substrate or some other substrate assembly atop monocrystalline silicon or some other material. A crystalline material of a first crystalline phase 34, such as a refractory metal silicide, is formed outwardly of substrate 32. An example technique, as with the above described embodiment, is by chemical vapor deposition. Alternate examples of providing first phase crystalline materials for layers 14, 24 and 34 of the first described embodiments will be described below. Compressive stress inducing atoms 36 are provided within first crystalline phase material layer 34. Where layer 34 comprises a refractory metal silicide, atoms 36

1 advantageously are provided to be larger than silicon atoms of the
2 silicide to produce desired compressive stress during the anneal to
3 produce the volume reduced phase transformation. Such example atoms
4 include Ge, W and Co or mixtures thereof. One example technique for
5 providing atoms 36 within layer 34 is by ion implantation or gas
6 diffusion. An example concentration range is from 10^{16} - 10^{22}
7 atoms/cm³.

8 Referring to Fig. 6, the refractory metal silicide of the first
9 crystalline phase is annealed under conditions effective to transform
10 silicide to a more dense second crystalline phase layer 35, with
11 atoms 36 inducing compressive stress during such anneal. Anneal
12 conditions as described above are preferred.

13 Thus, the above described embodiments provide alternate examples
14 of providing stress inducing material proximate (either within or
15 operatively adjacent) a crystalline material of a first crystalline phase
16 which is to undergo phase transformation to a second crystalline phase.
17 In the described and preferred embodiment, such is accompanied by a
18 volume reduction such that the stress induced is desirably of a
19 compressive nature. The above two techniques could of course also be
20 combined such that the stress inducing material is provided both within
21 and operatively adjacent the material undergoing phase transformation.
22 Further, the stress inducing material layer might be provided prior to
23 the subject layer being transformed being at the first crystalline phase
24 conditions. For example, refractory metals when deposited over silicon

1 containing layers, such as polysilicon, undergo chemical transformation
2 to silicides merely under elevated temperature anneal conditions. In
3 each of the above described embodiments, the stress inducing material
4 was provided after the silicide material of the first crystalline phase
5 came into existence. An alternate example whereby the stress inducing
6 material is provided before the first phase crystalline material comes
7 into existence is initially described with reference to Fig. 7 - 9.

8 Fig. 7 illustrates a wafer fragment 38 comprised of a substrate in
9 the illustrated form of a silicon, SiO_2 or other material substrate 40
10 having an overlying stress inducing material layer 42, such as SiO_2 or
11 Si_3N_4 . An example thickness for layer 42 is from 100 - 2000
12 Angstroms. A polysilicon layer 44 of an example thickness of from 100
13 - 2000 Angstroms is provided outwardly of stress inducing material
14 layer 44. Outwardly thereof is provided a refractory metal layer 46,
15 such as elemental titanium. Thus, a refractory metal (i.e., layer 46) is
16 formed on a silicon containing substrate (i.e. layer 44). The thickness
17 of layer 42 is preferably greater than or equal to the combined
18 thickness of layers 44 and 46.

19 Referring to Fig. 8, wafer 38 is annealed to impart a reaction to
20 form a refractory metal silicide layer 48 of, for example, the first C49
21 crystalline phase from the refractory metal of layer 46 and the silicon
22 of the underlying substrate 44. Example anneal conditions include
23 600°C , 760 Torr in an inert N_2 or Ar ambient for 20 seconds.

Referring to Fig. 9, refractory metal silicide layer 48 of the first crystalline phase is annealed to transform the first phase silicide to a more dense second crystalline phase layer 49. Example anneal conditions for such phase transformation are as described above with respect to the first described embodiments. Alternately, the wafer fragment of Fig. 7 could inherently be subjected to the second phase transformation anneal conditions at the outset, wherein the wafer being processed would inherently be transformed initially to the Fig. 8 embodiment and subsequently to the Fig. 9 embodiment.

The above described embodiment with respect to Figs. 7 - 9 could of course also be utilized in conjunction with the Figs. 5 and 6 embodiment wherein the stress inducing material is provided within the first crystalline phase material. For example, the compressive stress inducing atoms can be provided *in situ* into a refractory metal layer during its deposition over an underlying silicon containing substrate. Such could be provided for example by sputtering or chemical vapor deposition such that the atoms are received within the deposited refractory metal layer. Alternately, ion implanting or gas diffusion doping could be utilized. An example concentration range for the stress inducing atoms is as described above, namely from 10^{16} - 10^{22} atoms/cm³. Subsequently, the refractory metal layer having the atoms therein would be annealed to form the refractory metal silicide of the first crystalline phase from the reaction of the refractory metal and underlying silicon. Continued or subsequent annealing with the stress

1 inducing atoms in place will facilitate phase transformation to the
2 second phase.

3 Another alternate embodiment is described with reference to
4 Figs. 10-12 whereby the stress inducing layer is provided over or
5 outwardly of, and thereby operatively adjacent, the titanium layer prior
6 to its initial transformation to the first C49 crystalline phase. Fig. 10
7 illustrates a semiconductor wafer fragment 50 comprised of a bulk
8 monocrystalline silicon substrate and an overlying insulating layer 54,
9 such as SiO_2 . A polysilicon layer 56 is provided outwardly of layer 54,
10 with a refractory metal layer 58, such as titanium, provided outwardly
11 of polysilicon layer 56. A compressive stress inducing layer 60 is
12 provided over and on titanium layer 58 and preferably has a thickness
13 equal to or greater than the combined thickness of layers 56 and 58.

14 Referring to Fig. 11, suitable annealing conditions for example as
15 described above are utilized to transform layers 56 and 58 into a C49
16 first crystalline phase layer 61.

17 Referring to Fig. 12, subsequent or continued suitable annealing
18 transforms first crystalline phase material layer 61 into second C54
19 crystalline phase material layer 63, with the presence of compressive
20 stress inducing layer 60 facilitating such phase transformation as
21 described above.

22 The above described embodiments can be utilized in contact or
23 any other technologies where refractory metal silicides or other
24 crystalline materials are formed. An example embodiment in utilizing

aspects of the above process in fabricating of electrically conductive lines is described with reference to Figs. 13 - 16.

Referring to Fig. 13, a wafer fragment 65 comprises a bulk monocrystalline silicon substrate 66 having a gate oxide layer 68 provided thereover. A layer of polysilicon 70 is provided outwardly of gate oxide layer 68 with a silicide layer 72 of a C49 first crystalline phase provided outwardly of polysilicon layer 70. Such can be provided by the above or other conventional techniques. Thus, a semiconductive material (i.e. silicon of layer 70) is provided over a substrate, (i.e. material 68 and 66), with a refractory metal silicide 72 of a first crystalline phase being provided over and in ohmic electrical connection with the semiconductive materials. Layer 70 is desirably conductively doped with a suitable conductively enhancing impurity either at this point or subsequent in the processing.

Referring to Fig. 14, layers 72, 70 and 68 are patterned into conductive lines 74 and 76.

Referring to Fig. 15, a compressive stress inducing material layer 78 is formed outwardly of lines 74 and 76, preferably to a thickness at least as great as silicide portion 72. Again, preferred materials include SiO_2 or Si_3N_4 .

Referring to Fig. 16, the wafer fragment is annealed as above to transform the silicide material 72 of the first crystalline phase to C54 second crystalline phase material 80. Layer 78 can remain, be removed,

1 anisotropically etched or otherwise processed as the circuitry design
2 dictates.

3 The above described Figs. 13-16 embodiment is a technique
4 whereby the conductive line patterning (in this example a gate line) is
5 conducted before the annealing, and the compressive stress inducing
6 material is provided after the line patterning. Alternately, the
7 patterning can be conducted after the annealing. Further, compressive
8 stress inducing material can be provided within the first crystalline phase
9 refractory metal silicide layer 72 as is for example described with
10 reference to the Figs. 5 and 6 embodiment. Alternate techniques are
11 also of course contemplated, as will be appreciated by the artisan.

12 A further alternate embodiment is described with reference to
13 Figs. 17 - 19. Fig. 17 illustrates a semiconductor wafer fragment 83
14 (such as monocrystalline silicon) having opposing first and second sides
15 84 and 85, respectively.

16 Referring to Fig. 18, a crystalline material layer 87 of a first
17 crystalline phase (such as the exemplary C49 TiSi_x) is formed over first
18 wafer side 84. A compressive stress inducing material layer 89 is
19 provided over and on second wafer side 85. Layer 89 is provided to
20 have a thermal coefficient of expansion which exceeds that of layer 87.
21 An example material where layer 87 comprises a refractory metal silicide
22 is TiN.

23 Referring to Fig. 19, wafer 83 is annealed under conditions such
24 as that described above to transform first phase material 87 into second

1 phase material 91. The greater coefficient of layer 89 as compared to
2 layer 87 causes a degree of bowing which effectively places layer 87 in
3 compressive stress to facilitate its transformation to layer 91.

4 In compliance with the statute, the invention has been described
5 in language more or less specific as to structural and methodical
6 features. It is to be understood, however, that the invention is not
7 limited to the specific features shown and described, since the means
8 herein disclosed comprise preferred forms of putting the invention into
9 effect. The invention is, therefore, claimed in any of its forms or
10 modifications within the proper scope of the appended claims
11 appropriately interpreted in accordance with the doctrine of equivalents.
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CLAIMS:

1. A method of forming a crystalline phase material comprising:
providing a stress inducing material operatively adjacent a
crystalline material of a first crystalline phase, the stress inducing
material having a first thermal coefficient of expansion, the crystalline
material of the first crystalline phase having a second thermal coefficient
of expansion, the first coefficient being less than the second coefficient;
and

annealing the crystalline material of the first crystalline phase
under conditions effective to transform it to a second crystalline phase.

2. The method of claim 1 comprising providing the stress
inducing material over the first crystalline phase material.

3. The method of claim 1 comprising providing the stress
inducing material under the first crystalline phase material.

4. The method of claim 1 comprising providing the stress
inducing material to a thickness which is equal to or greater than a
thickness of the first phase crystalline material.

5. The method of claim 1 comprising providing the stress inducing material over and in contact with the first crystalline phase material.

6. The method of claim 1 comprising providing the stress inducing material under and in contact with the first crystalline phase material.

7. The method of claim 1 wherein the stress inducing material comprises SiO_2 .

8. The method of claim 1 wherein the stress inducing material comprises Si_3N_4 .

9. The method of claim 1 wherein the stress inducing material is provided before said annealing.

10. A method of lowering required activation energy in transforming a crystalline material from a first crystalline phase to a more dense second crystalline phase comprising providing a compressive stress inducing material operatively adjacent the material of the first crystalline phase during an anneal to the second crystalline phase, with the compressive stress inducing material having a first thermal coefficient of expansion, the crystalline material of the first crystalline phase having a second thermal coefficient of expansion, the first coefficient being less than the second coefficient.

11. A method of forming a crystalline phase material comprising: providing a semiconductor wafer having opposing first and second sides;

forming a crystalline material of a first crystalline phase over the first side of the wafer;

forming a stress inducing material over the second side of the wafer, the stress inducing material having a first thermal coefficient of expansion, the crystalline material of the first crystalline phase having a second thermal coefficient of expansion, the first coefficient being greater than the second coefficient; and

annealing the crystalline material of the first crystalline phase under conditions effective to transform it to a second crystalline phase.

12. The method of claim 11 comprising forming the stress inducing material on the second side of the wafer.

13. The method of claim 11 wherein the crystalline material comprises a refractory metal silicide, and the stress inducing material comprises TiN.

14. The method of claim 11 wherein the crystalline material comprises TiSi_x , the first crystalline phase is C49, the second crystalline phase is C54, and the stress inducing material comprises TiN.

15. The method of claim 11 wherein the crystalline material comprises TiSi_x , the first crystalline phase is C49, and the second crystalline phase is C54

16. The method of claim 11 wherein the stress inducing material is provided before said annealing.

17. A method of forming a crystalline phase material comprising: providing a stress inducing material within a crystalline material of a first crystalline phase; and

annealing the crystalline material of the first crystalline phase under conditions effective to transform it to a second crystalline phase.

18. The method of claim 17 comprising ion implanting the stress inducing material into the first crystalline phase material.

19. The method of claim 17 comprising *in situ* providing the stress inducing material into the first crystalline phase material during deposition of the first crystalline phase material.

20. The method of claim 17 comprising providing stress inducing atoms within the first crystalline phase material to a concentration from 10^{16} - 10^{22} atoms/cm³.

21. A method of forming a refractory metal silicide comprising:
forming a refractory metal silicide of a first crystalline phase;
providing compressive stress inducing atoms within the refractory metal silicide of the first crystalline phase, the compressive stress inducing atoms being larger than silicon atoms of the silicide; and

with the compressive stress inducing atoms within the first phase refractory metal silicide, annealing the refractory metal silicide of the first crystalline phase under conditions effective to transform said silicide to a more dense second crystalline phase.

1 22. The method of claim 21 wherein the refractory metal silicide
2 comprises TiSi_x , and the first crystalline phase is C49 and the second
3 crystalline phase is C54.

4
5 23. The method of claim 21 comprising ion implanting the
6 compressive stress inducing atoms into the first crystalline phase
7 refractory metal silicide.

8
9 24. The method of claim 21 comprising *in situ* providing the
10 compressive stress inducing atoms into a refractory metal layer during
11 deposition of said refractory metal layer over an underlying silicon
12 containing substrate; and

13 annealing the refractory metal layer to form said refractory metal
14 silicide of the first crystalline phase from the refractory metal and
15 silicon of the underlying substrate.

16
17 25. The method of claim 21 wherein the compressive stress
18 inducing atoms are selected from the group consisting of Ge, W and
19 Co, or mixtures thereof.

20
21 26. The method of claim 21 comprising providing the atoms to
22 a concentration within the refractory metal silicide from 10^{16} - 10^{22}
23 atoms/cm³.

1 27. A method of forming an electrically conductive line
2 comprising:

3 forming a semiconductive material over a substrate;

4 forming a refractory metal silicide of a first crystalline phase over
5 and in ohmic electrical connection with the semiconductive material;

6 providing a compressive stress inducing material proximate the
7 refractory metal silicide of the first crystalline phase;

8 after providing the compressive stress inducing material, annealing
9 the refractory metal silicide of the first crystalline phase to transform
10 said silicide to a more dense and more electrically conductive second
11 crystalline phase; and

12 patterning the semiconductive material and the refractory metal
13 silicide into a conductive line.

14
15 28. The method of claim 27 wherein the compressive stress
16 inducing material is provided within the refractory metal silicide of the
17 first crystalline phase.

18
19 29. The method of claim 27 wherein the compressive stress
20 inducing material is provided operatively adjacent the refractory metal
21 silicide of the first crystalline phase.
22
23
24

1 30. The method of claim 27 wherein the patterning is conducted
2 before the annealing.

3
4 31. The method of claim 27 wherein the patterning is conducted
5 before the annealing, and the compressive stress inducing material is
6 provided after the patterning.

7
8 32. The method of claim 27 wherein the patterning is conducted
9 after the annealing.

10
11 33. The method of claim 27 wherein the refractory metal silicide
12 comprises TiSi_x , and the first crystalline phase is C49 and the second
13 crystalline phase is C54.

14
15 34. The method of claim 27 comprising providing the
16 compressive stress inducing material over the first crystalline phase
17 refractory metal silicide.

18
19 35. The method of claim 27 comprising providing the
20 compressive stress inducing material over the first crystalline phase
21 refractory metal silicide, the compressive stress inducing material having
22 a thickness equal to or greater than a thickness of the first phase
23 refractory metal silicide.
24

1 36. The method of claim 27 comprising providing the
2 compressive stress inducing material under the first crystalline phase
3 refractory metal silicide.

4
5 37. The method of claim 27 wherein the compressive stress
6 inducing material comprises SiO_2 .

7
8 38. The method of claim 27 wherein the compressive stress
9 inducing material comprises Si_3N_4 .

10
11 39. The method of claim 27 wherein the compressive stress
12 inducing material is provided both in and operatively adjacent the first
13 phase crystalline silicide.

40. A method of forming a refractory metal silicide comprising:
forming a refractory metal on a silicon containing substrate;
providing a compressive stress inducing material proximate the
refractory metal;

after providing the compressive stress inducing material, annealing
the refractory metal to form a refractory metal silicide of a first
crystalline phase from the refractory metal and silicon of the underlying
substrate; and

annealing the refractory metal silicide of the first crystalline phase
to transform the first phase silicide to a more dense second crystalline
phase.

41. The method of claim 40 wherein the refractory metal silicide
comprises TiSi_x , and the first crystalline phase is C49 and the second
crystalline phase is C54.

42. The method of claim 40 comprising providing the
compressive stress inducing material within the first crystalline phase
refractory metal silicide.

43. The method of claim 40 comprising providing the
compressive stress inducing material over the first crystalline phase
refractory metal silicide.

44. The method of claim 40 comprising providing the compressive stress inducing material over the first crystalline phase refractory metal silicide to a thickness equal to or greater than a thickness of the first phase refractory metal silicide.

45. The method of claim 40 comprising providing the compressive stress inducing material under the first crystalline phase refractory metal silicide.

46. A method of forming a crystalline phase material comprising:
forming a crystalline material of a first crystalline phase over a substrate;

forming a layer over the first phase crystalline material; and

after forming the layer, annealing the crystalline material of the first crystalline phase under conditions effective to transform it to a second crystalline phase.

47. The method of claim 46 wherein the crystalline material comprises TiSi_x , the first crystalline phase is C49, and the second crystalline phase is C54

1 48. A method of forming a crystalline phase material comprising:
2 forming a crystalline material of a first crystalline phase over a
3 substrate;

4 providing dopant atoms to within the first phase crystalline
5 material; and

6 after providing the dopant atoms, annealing the crystalline material
7 of the first crystalline phase under conditions effective to transform it
8 to a second crystalline phase.

9
10 49. The method of claim 48 wherein the crystalline material
11 comprises TiSi_x , the first crystalline phase is C49, and the second
12 crystalline phase is C54

13
14 50. The method of claim 48 wherein the providing comprises ion
15 implanting.

16
17 51. The method of claim 48 wherein the providing comprises gas
18 diffusion doping.

1 ABSTRACT OF THE DISCLOSURE

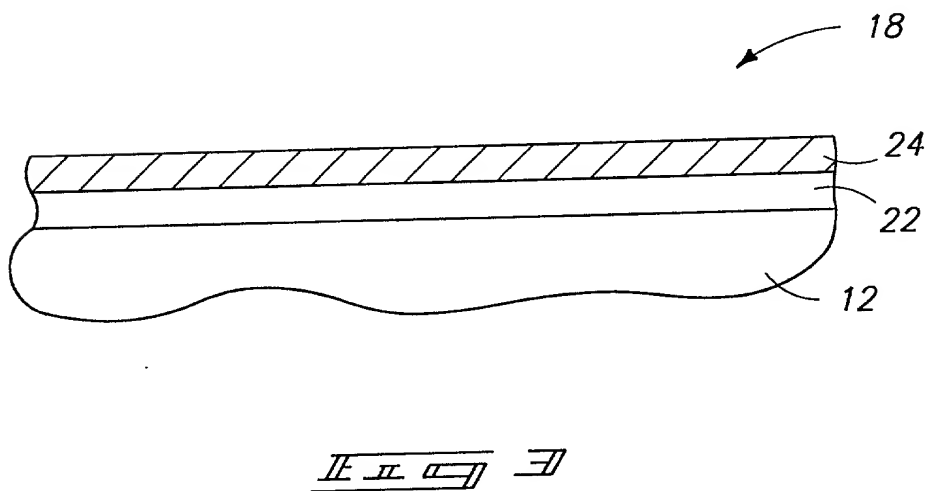
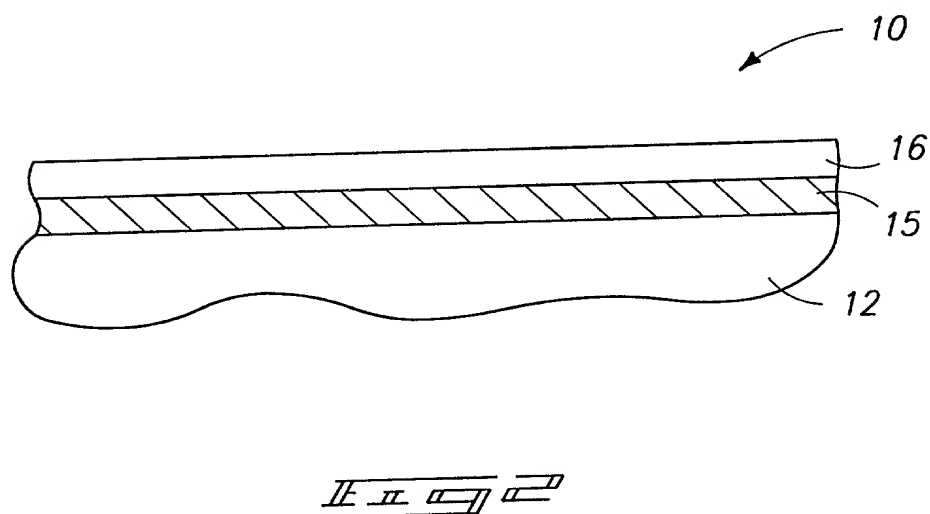
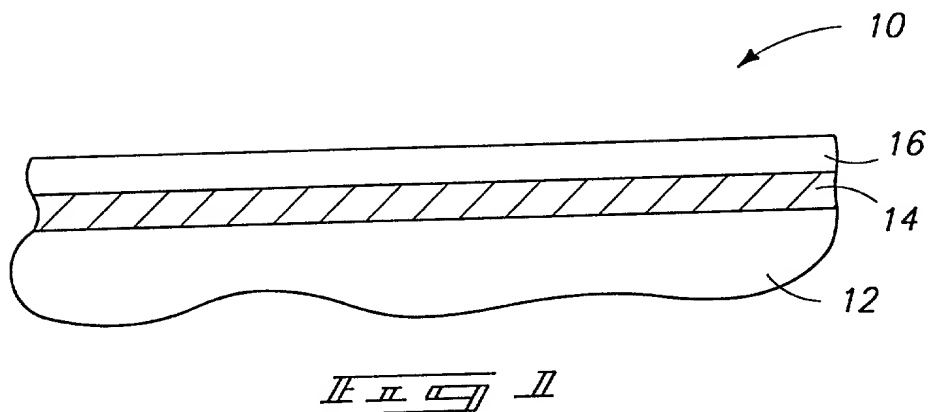
2 A method of forming a crystalline phase material includes,
3 a) providing a stress inducing material within or operatively adjacent a
4 crystalline material of a first crystalline phase; and b) annealing the
5 crystalline material of the first crystalline phase under conditions
6 effective to transform it to a second crystalline phase. The stress
7 inducing material preferably induces compressive stress within the first
8 crystalline phase during the anneal to the second crystalline phase to
9 lower the required activation energy to produce a more dense second
10 crystalline phase. Example compressive stress inducing layers include
11 SiO₂ and Si₃N₄, while example stress inducing materials for providing
12 into layers are Ge, W and Co. Where the compressive stress inducing
13 material is provided on the same side of a wafer over which the
14 crystalline phase material is provided, it is provided to have a thermal
15 coefficient of expansion which is less than the first phase crystalline
16 material. Where the compressive stress inducing material is provided
17 on the opposite side of a wafer over which the crystalline phase
18 material is provided, it is provided to have a thermal coefficient of
19 expansion which is greater than the first phase crystalline material.
20 Example and preferred crystalline phase materials having two phases are
21 refractory metal silicides, such as TiSi_x.

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24

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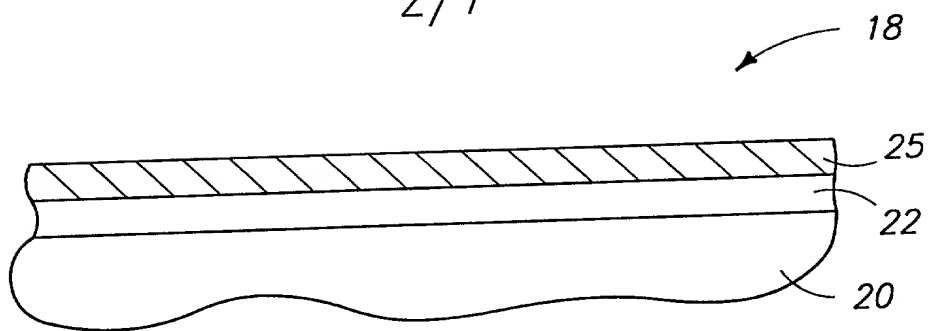


FIG. 4

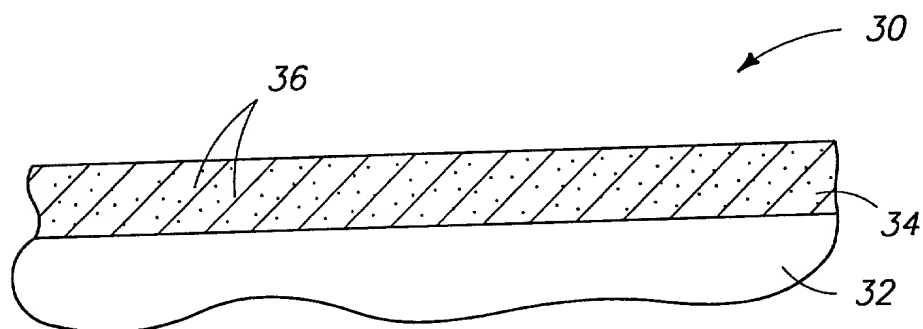


FIG. 5

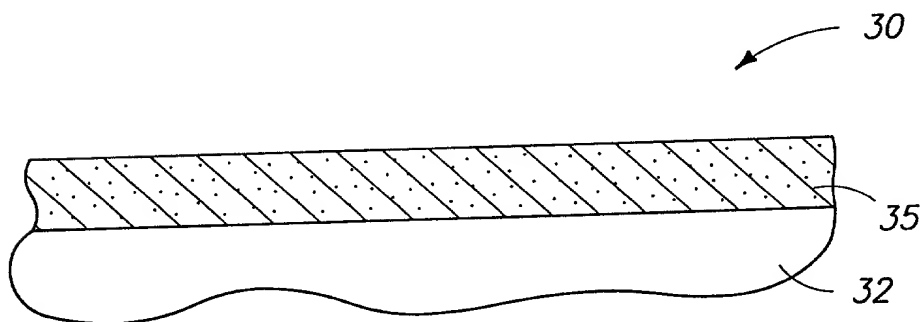


FIG. 6

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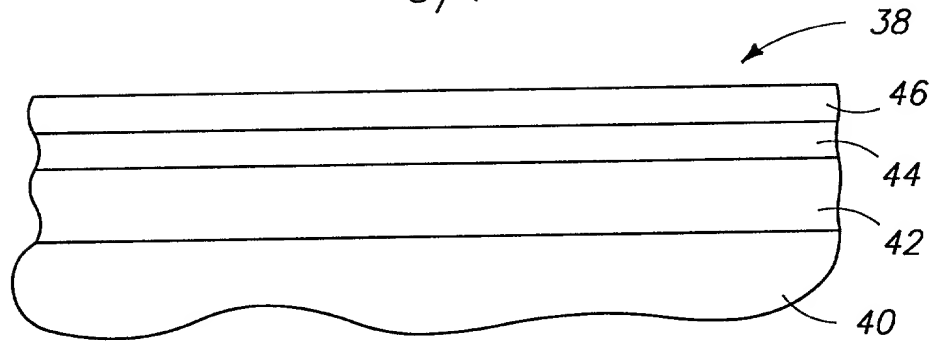


FIG. 3

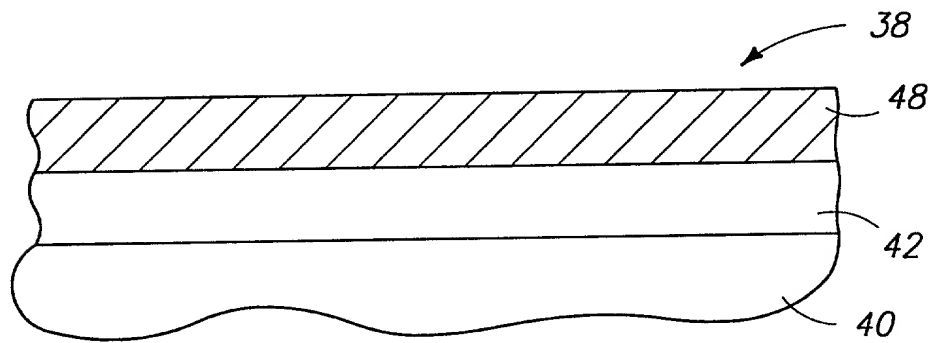


FIG. 4

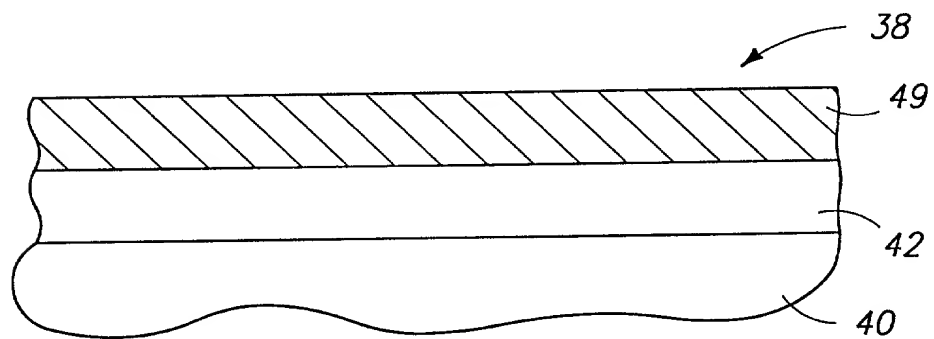


FIG. 5

FIG. 3

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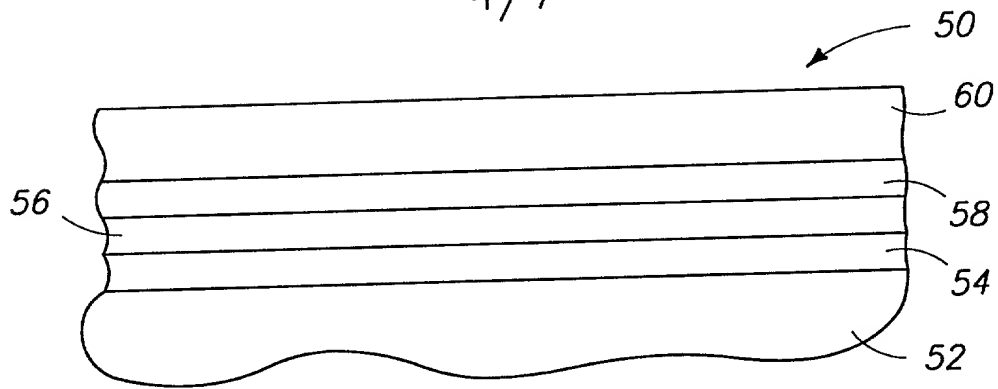


FIG. 100

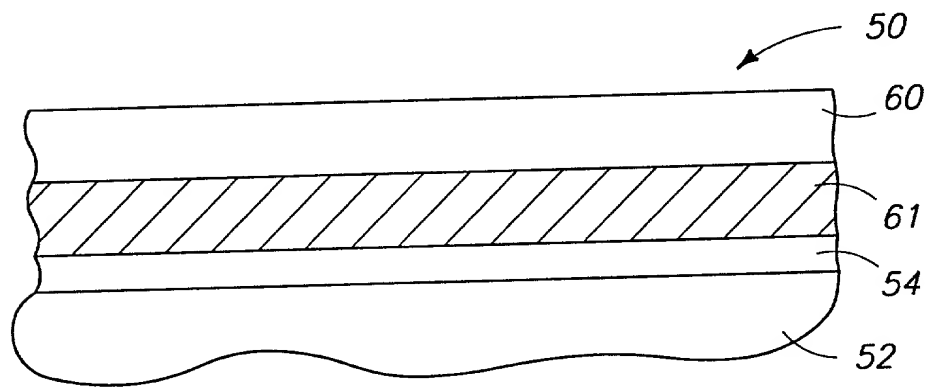


FIG. 111

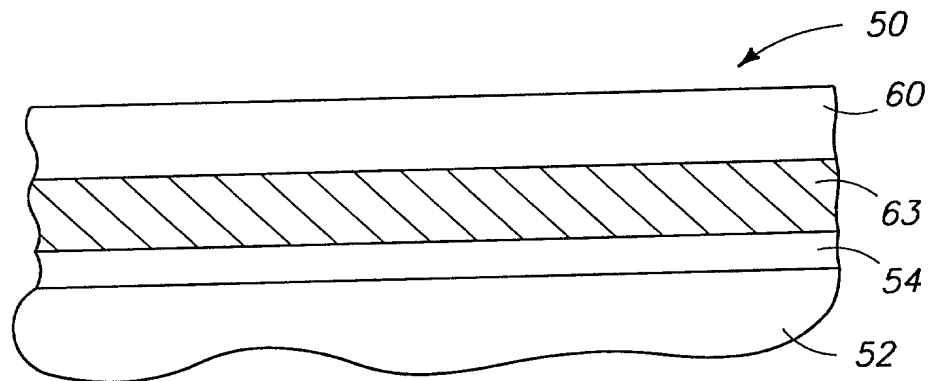


FIG. 120

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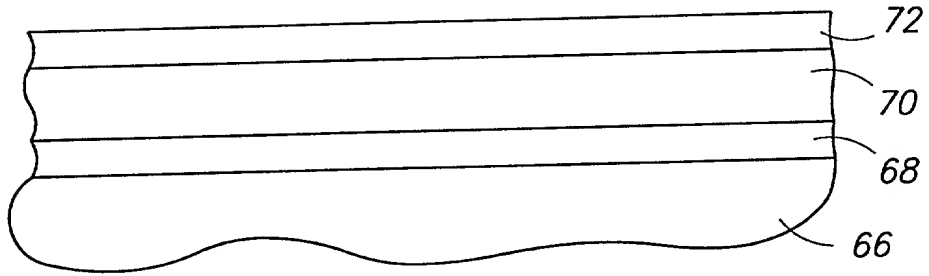


FIG. 1

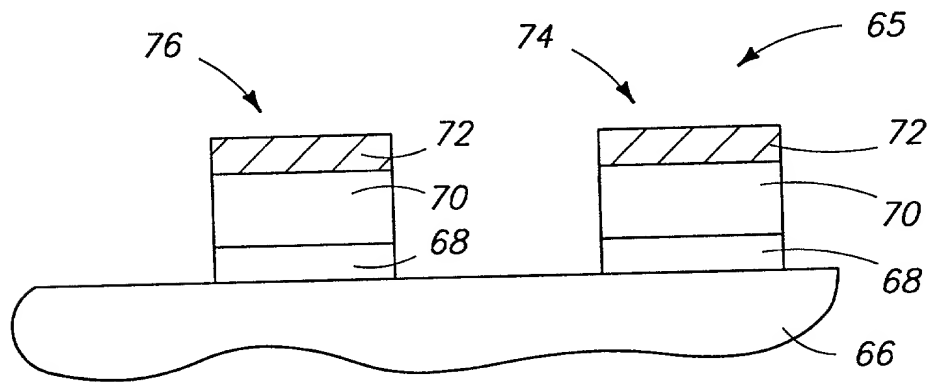


FIG. 2

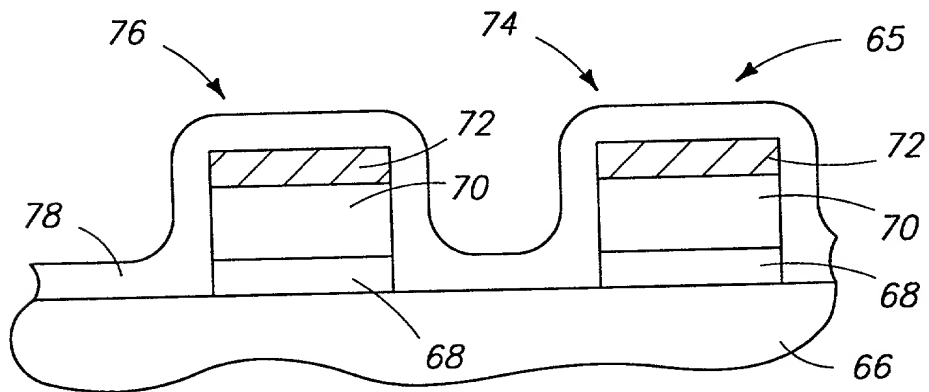


FIG. 3

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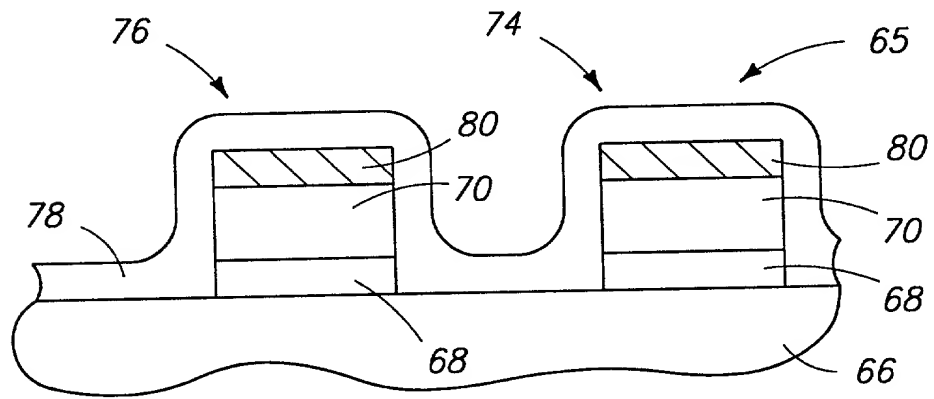
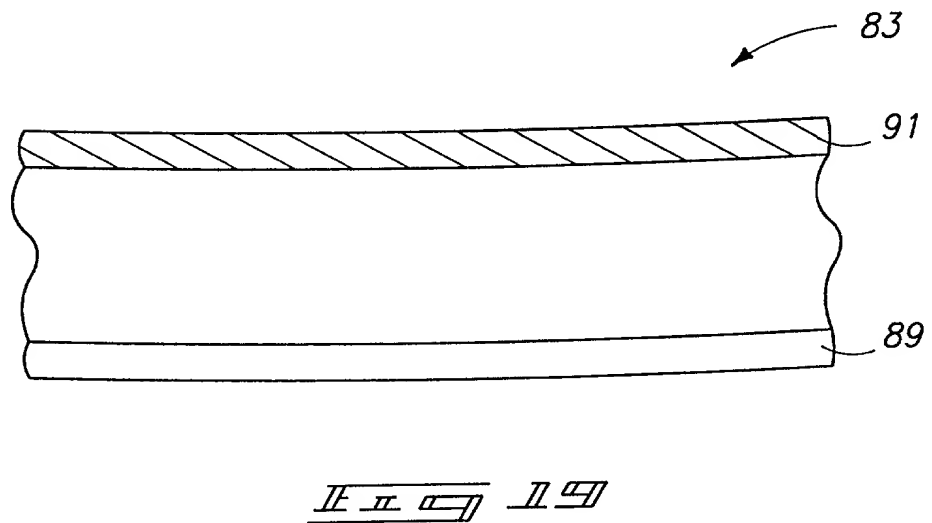
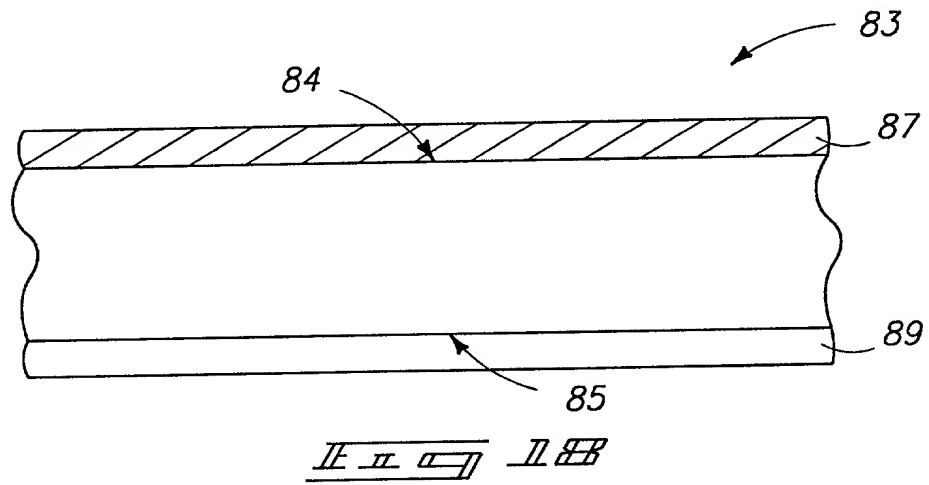
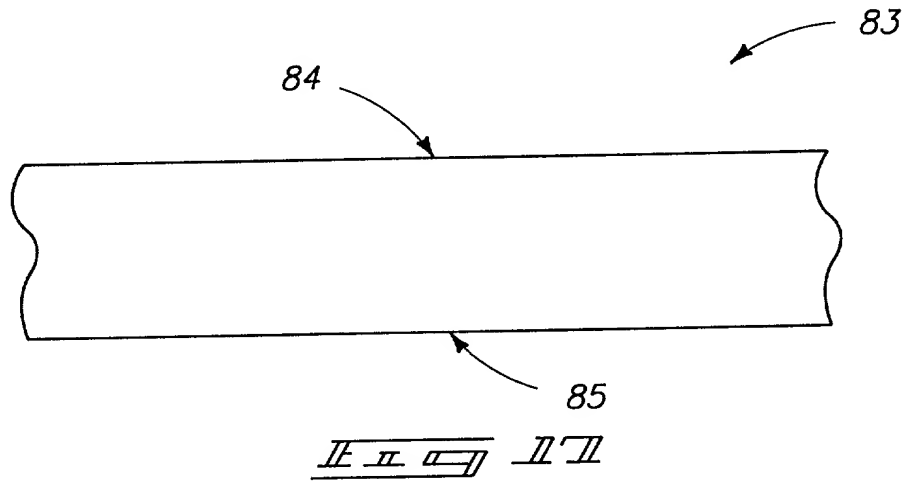


FIG. 11

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DECLARATION OF JOINT INVENTORS FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: Method Of Forming A Crystalline Phase Material, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

PRIOR FOREIGN APPLICATIONS:

I hereby state that no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

POWER OF ATTORNEY:

As a named Inventor, I hereby appoint the following attorneys and agent to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: Richard J. St. John, Reg. No. 19,363; David P. Roberts, Reg. No. 23,032; Randy A. Gregory, Reg. No. 30,386; Mark S. Matkin, Reg. No. 32,268; James L. Price, Reg. No. 27,376; Deepak Malhotra, Reg. No. 33,560; Mark W. Hendricksen,

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5 Michael L. Lynch, Reg. No. 30,871.

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8 WA 99204-0317. Direct telephone calls to: Mark S. Matkin,
9 (509) 624-4276.

10 I hereby declare that all statements made herein of my own
11 knowledge are true and that all statements made on information and
12 belief are believed to be true; and further that these statements were
13 made with the knowledge that willful false statements and the like so
14 made are punishable by fine or imprisonment, or both, under
15 Section 1001 of Title 18 of the United States Code and that such willful
16 false statement may jeopardize the validity of the application or any
17 patent issued therefrom.

* * * * *

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